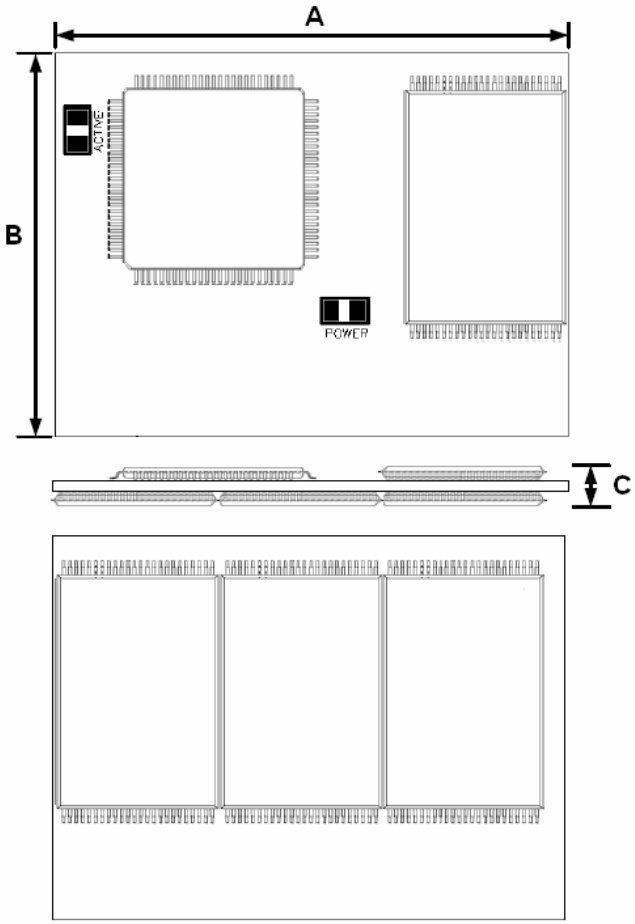
TS2GIFD10 / TS4GIFD10 / TS8GIFD10
TS2GIFD10M / TS4GIFD10M / TS8GIFD10M 1" IDE FLASH DISK

Description

The 1-inch IDE Flash Disk is small in size, has a huge capacity and low power consumption making it perfect for use as a mobile storage solution in devices such as, Mobile Phones, PDA and GPS systems. This guide is written to provide general installation and handling information, please use it in conjunction with the Owner's Manual for your device or system.

Placement



Features

- RoHS compliant
- Fully compatible with 1.0-inch hard drive form factor and interface
- Non-volatile Flash Memory for outstanding data retention
- Built-in ECC (Error Correction Code) functionality and wear-leveling algorithm ensures highly reliable of data transfer
- Supports up to PIO Mode 6 and Ultra DMA Mode 4
- LED indicates usage status (Power and Data Access)
- Lower Power Consumption
- Shock resistance

Dimensions

Side	Millimeters	Inches
A	40.00 ± 0.30	1.575 ± 0.012
B	30.00 ± 0.20	1.181 ± 0.008
C	3.50 ± 0.50	0.138 ± 0.020

Specifications

Physical Specification		
Form Factor		1-inch HDD
Storage Capacities		2 GB to 8 GB
Dimensions (mm)	**Length**	30.0 0 ± 0.20
	Width	40.00 ± 0.30
	Height	3.50 ± 0.50
Weight		6 g

Environmental Specifications	
Operating Temperature	0 ℃ to 70 ℃
Storage Temperature	- 40 ℃ to 85 ℃

Reliability	
Write/Erase Endurance*	> 2,000,000 cycles
Read Endurance	Unlimited
Data Reliability	Built-in 4 symbol correction ECC (per 512 bytes Sector)
Connector Durability	10,000 times

* Note: Base on SLC Flash.

Interface Specification	
Jumper Settings	No Jumper Setting (**Default: Master mode**)
Drivers	No Device Driver Required
ATA Compatibility	ATA/ATAPI 5
	* PIO Modes 0 – 6
	Ultra DMA Modes 0 - 4

* Note: There is no -IOCS16 signal support and all Data Transfer is 16-bits in width.

Compliance and Warranty	
Compliance	CE, FCC and BSMI
Warranty	2 years

Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name
01	GND	02	DD10
03	DD9	04	DD2
05	DD8	06	DD1
07	-PDIAG : -CBLID	08	DD0
09	-DASP	10	DA0
11	-DMACK	12	DA1
13	DMARQ	14	DA2
15	IORDY : DDMARDY : DSTROBE	16	-RESET
17	-CSEL	18	VCC
19	VCC	20	INTRQ
21	-DIOW : STOP	22	-DIOR : -HDMARDY : HSTROBE
23	-CS1	24	-CS0
25	DD15	26	DD7
27	DD14	28	DD6
29	DD13	30	DD5
31	DD12	32	DD4
33	DD11	34	DD3
35	GND		

Pin Description

Pin No.	Signal	I/O*	Description
24, 23	-CS0, -CS1 (Chip select)	I	These signals are used to select the Command Block and Control Block registers. When –DMACK is asserted, -CS0 and –CS1 shall be negated and transfers shall be 16 bits wide.
10, 12, 14	DA0 ~ DA2 (Device Address)	I	This is the 3-bit binary coded Address Bus.
9	-DASP (Device active)	I/O	The device asserts this signal when active. The device will not be Device 1. During the reset protocol, the device will not assert this signal.
2~6, 8, 25~34	DD0 ~ DD15 (Device Data)	I/O	These signals are 16 bits bi-direction Data Bus between the host and the device. The DD(7:0) are used for 8-bit register transfers and ECC access.
22	-DIOR (I/O Read)	I	This is the strobe signal used by the host to read device registers or the Data port.
	-HDMARDY (UDMA ready)		This is a flow control signal for Ultra DMA data-in bursts. This signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY- to pause an Ultra DMA data-in burst.
	HSTROBE (UDMA Strobe)		This is the data-out strobe signal from the host for an Ultra DMA data-out burst. Both the rising and falling edge of HSTROBE latch the data from DD(15:0) into the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
21	-DIOW (Device I/O Write)	I	This is the strobe signal asserted by the host to write to the device register or the Data port.
	STOP (Stop UDMA Burst)		This signal shall be negated by the host prior to initiation of an Ultra DMA burst. Assertion of STOP by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.
11	-DMACK (DMA acknowledge)	I	This signal is used by the host in response to DMARQ to initiate DMA transfer.
13	DMARQ (DMA Request)	O	For DMA data transfers. Device will assert DMARQ when the device is ready to transfer data to or from the host.
7	-PDIAG (Pass diagnostics)	I/O	Optional signal: The device will only be a Device 0. This signal may be asserted by Device 1 to indicate to Device 0 that Device 1 has completed diagnostics. Leave disconnected if not used.
16	-RESET	I	Hardware reset signal from the host.

15	IORDY (I/O channel ready)	O	This signal is used to temporarily stop the host register access (read or write) when the device is not ready to respond to a data transfer request.
	DDMARDY (UDMA ready)		The device will assert this signal to indicate that the device is ready to receive Ultra DMA data-out burst.
	DSTROBE (UDMA data strobe)		When Ultra DMA mode DMA Read is active, this signal is the data-in strobe generated by the device.
17	CSEL (Cable select) Default: Not support	I	This pin is used to configure this device as Device 0 or Device 1. When this pin is grounded, this device is configured as Device 0. When this pin is High, this device is configured as Device 1.
20	INTRQ (Interrupt)	O	When this device is selected, this signal is the active high Interrupt Request to the host.
18, 19	VCC	P	Power supply.
01, 35	GND	-	Ground.

* Note:

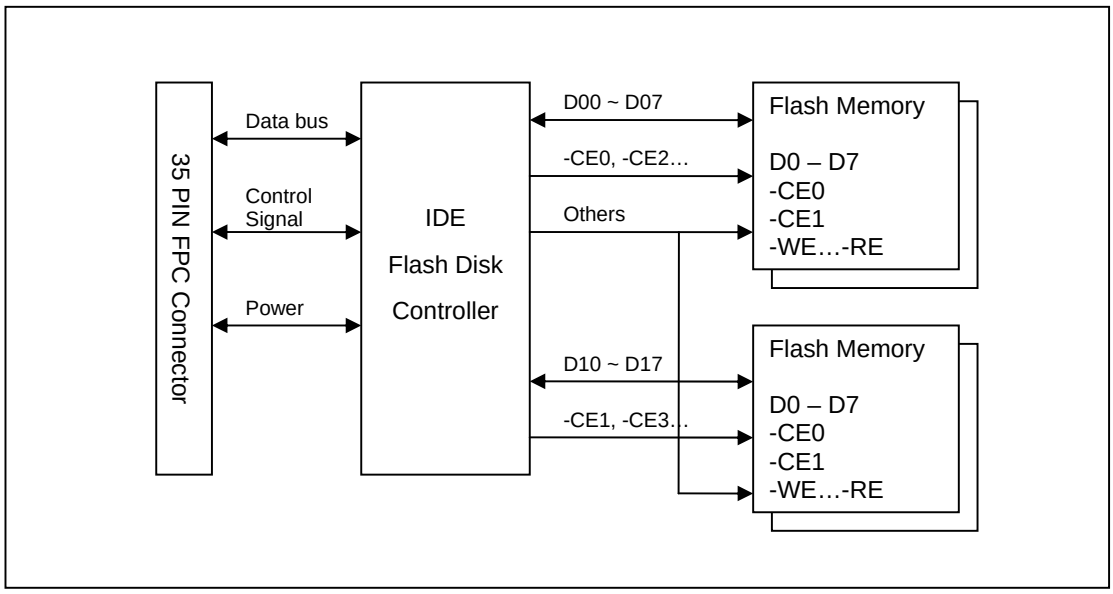
"**I**" An input from the host system to the device.

"**O**" An output from the device to the host system.

"**I/O**" An input/output (bi-direction) common.

"**P**" Power supply.

Block Diagram



DC Characteristics

Symbol	Description	Min	Max	Units
I_{oL}	Driver sink current	4		mA
I_{oLDASP}	Driver sink current for DASP	12		mA
I_{oH}	Driver source current	400		µA
$I_{oHDMARQ}$	Driver source current for DMARQ	500		µA
I_Z	Device pull-up current on DD(15:0) and STROBE when released	-10	200	µA
V_{iH}	Voltage input high	2.0	5.5	V
V_{iL}	Voltage input low		0.8	V
V_{oH}	Voltage output high at I_{oH} min	2.4		V
V_{oL}	Voltage output low at I_{oL} min		0.5	V

AC Characteristics

Symbol	Description	Min	Max	Units
S_{RISE}	Rising edge slew rate for any signal		1.25	V/ns
S_{FALL}	Falling edge slew rate for any signal		1.25	V/ns
C_{host}	Host interface signal capacitance at the host connector		25	pf
C_{device}	Device interface signal capacitance at the device connector		20	pf

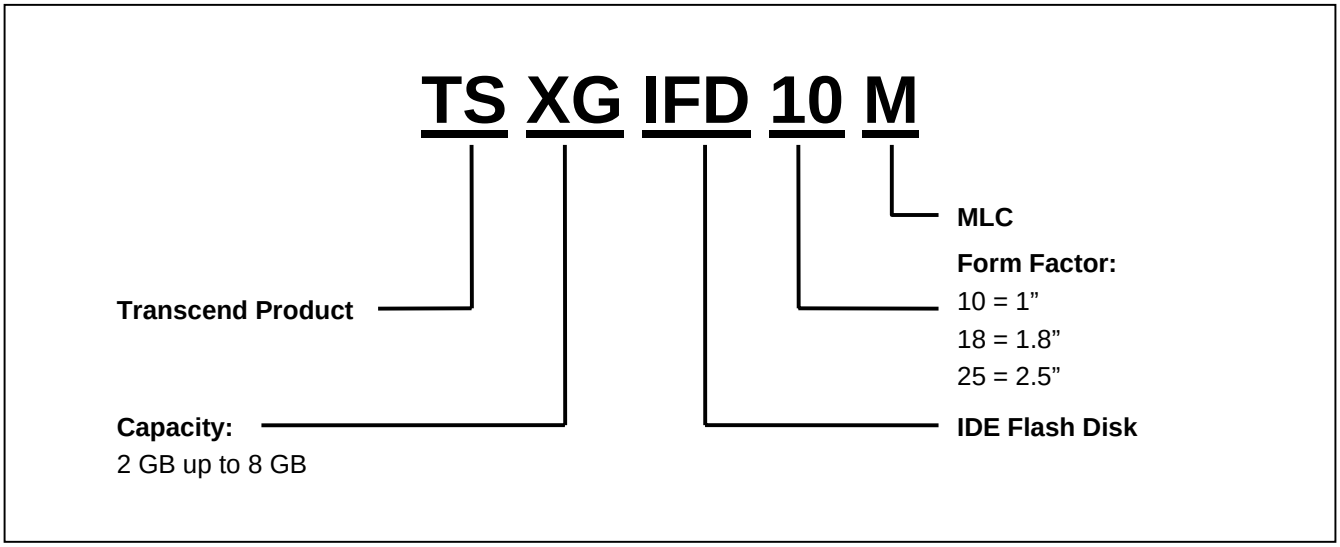
Command Set

The following table summarizes the command defined in the ATAPI-5 specification and lists the commands supported by the TS2/4/8GIFD10.

No.	Command set	Code	FR[1]	SC[1]	SN[1]	CY[1]	DR[1]	HD[1]	LBA[1]
1	CFA Erase Sector(s)	C0h	—	Y	Y	Y	Y	Y	Y
2	CFA Request Extended Error Code	03h	—	—	—	—	Y	—	—
3	CFA Translate Sector	87h	—	Y	Y	Y	Y	Y	Y
4	CFA Write Multiple w/o Erase	CDh	—	Y	Y	Y	Y	Y	Y
5	CFA Write Sector w/o Erase	38h	—	Y	Y	Y	Y	Y	Y
6	Check Power Mode	E5h	—	—	—	—	Y	—	—
7	Execute Device Diagnostic	90h	—	—	—	—	Y	—	—
8	Identify Device	ECh	—	—	—	—	Y	—	—
9	Idle	E3h	—	Y	—	—	Y	—	—
10	Idle Immediate	E1h	—	—	—	—	Y	—	—
11	Initialize Device Parameters	91h	—	Y	—	—	Y	Y	—
12	NOP	00h	—	—	—	—	Y	—	—
13	Read Buffer	E4h	—	—	—	—	Y	—	—
14	Read DMA	C8h	—	Y	Y	Y	Y	Y	Y
15	Read Multiple	C4h	—	Y	Y	Y	Y	Y	Y
16	Read Sector(s)	20h	—	Y	Y	Y	Y	Y	Y
17	Read Verify Sector(s)	40h	—	Y	Y	Y	Y	Y	Y
18	Seek	70h	—	—	Y	Y	Y	Y	Y
19	Set Features	EFh	Y	C	—	—	Y	—	—
20	Set Multiple Mode	C6H	—	Y	—	—	Y	—	—
21	Sleep	E6h	—	—	—	—	Y	—	—
22	Standby	E2h	—	—	—	—	Y	—	—
23	Standby Immediate	E0h	—	—	—	—	Y	—	—
24	Write Buffer	E8h	—	—	—	—	Y	—	—
25	Write DMA	CAh	—	Y	Y	Y	Y	Y	Y
26	Write Multiple	C5h	—	Y	Y	Y	Y	Y	Y
27	Write Sector	30h	—	Y	Y	Y	Y	Y	Y

Note 1: **FR** (Feature Register), **SC** (Sector Count Register), **SN** (Sector Number Register), **CY** (Cylinder Low/High Register), **DR** (Drive bit of Drive/Head Register), **HD** (Head No. bit0-bit3 of Drive/Head Register), **LBA** (Logical Block Address Mode supported). **Y**: Set up; —: Not set up; **C**: The register contains command specific data.

Ordering Information



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